AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 11, as follows:

Recently, the operation frequency of a semiconductor integrated circuit device has become very high. A wiring line region allocated for power supply wiring lines and ground wiring lines tends to have a greater increase in operation frequency. Therefore, it becomes easy for an internal circuit of the semiconductor integrated circuit device to be destroyed if a voltage [[serge]] surge is momentary applied or a high voltage is consistently applied when the semiconductor integrated circuit device is actually used. In order to avoid the destruction of the inner circuit due to application of the voltage [[serge]] surge or the high voltage, a protection circuit is conventionally connected with input/output terminals to improve the voltage endurance of the internal circuit. As one of such techniques, Japanese Laid Open Patent Application (JP-P2002-289704A) describes a technique, in which boron regions of different depths are formed as P-wells between two N-wells provided in a P-type substrate apart from each other. These regions are formed through two ion implantations using a same mask. The deeper boron region is deeper than the two N-wells to increase the breakdown voltage and to suppress leak between the two N-wells at the same time.

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